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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/625,386
Filing Date: July 23, 2003
Appellant(s): CHAUHAN, SUNDEEP

Mitchell K. McCarthy
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 11/21/2007 appealing from the Office action mailed 5/17/2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,249,693	Staszewski et al.	8-2002
6,351,154	Brachmann et al.	2-2002

Ruldolf F. Graf, "Modern Dictionary of Electronics", (February, 1999), page 258

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

Claims 1-3, 7, 10-12, 16, 17, 20-22, 25, 26 are rejected under 35 U.S.C. 102(e) as being anticipated by Staszewski et al. (US Pat. 6,429,693; hereinafter Staszewski).

With regard to claim 1, Staszewski discloses in Figs. 1-8 an apparatus comprising a phase/frequency comparator circuit (200) that is configured to generate a phase error (202) responsive to a transition location signal (604 as transition location signal before converted to TDC_RISE, TDC_FALL).

With regard to claim 7, the phase/frequency comparator further comprises a phase detecting stage that generates a result ($Q_{(0)}$-$Q_{(L-1)}$) that represents an instantaneous phase difference; and encoding circuitry (NORM) coupled to the phase detecting stage; wherein the

encoding circuitry converts a result of the phase detecting stage into a numerical phase difference value (PHF).

With regard to claim 2, the phase detecting stage further comprises a tapped delay line (502s) having a plurality of outputs and configured to receive a first signal (CKV); and a parallel latch coupled to the plurality of outputs of the tapped delay line and configured to receive a second signal (110), wherein the parallel latch stores the values of the plurality of outputs of the tapped delay line in response to a transition in the second signal; and wherein the encoding circuitry converts the values stored in the parallel latch into a numerical phase difference value.

With regard to claim 3, the phase/frequency comparator further comprises an accumulator (102) coupled to the encoding circuitry, wherein the accumulator adds the numerical phase difference value to a value stored in the accumulator to obtain an accumulated phase error (PHE).

With regard to claim 10, Staszewski discloses in Figs. 1-8 a phase locked loop comprising a controllable oscillator (103); and a phase/frequency comparator includes a phase detecting stage (201); encoding circuitry (NORM) coupled to the phase detecting stage; and an accumulator (102) coupled to the encoding circuitry.

With regard to claim 11, the phase detecting stage further comprises a tapped delay line (502s) having a plurality of outputs and configured to receive a first signal (CKV); and a parallel latch coupled to the plurality of outputs of the tapped delay line and configured to receive a second signal (110), wherein the parallel latch stores the values of the plurality of outputs of the tapped delay line in response to a transition in the second signal; and wherein the encoding

circuitry converts the values stored in the parallel latch into a numerical phase difference value (PHF).

Claim 12 is similarly rejected; note the above discussion with regard to claim 3.

With regard to claim 16, the forward path includes additional control circuitry (105).

With regard to claim 17, the reference also meets the recited limitation in the claim.

With regard to claim 20, Staszewski et al. discloses in Figs. 1-8 a corresponding method comprising the steps of generating a snapshot ($Q_{(0)}$-$Q_{(L-1)}$) of a first signal (114) in response to receiving a second signal (110); and mapping the snapshot to a numerical phase difference value (PHF) that is generated responsive to a signal that corresponds to a transition location of the first signal (604 as transition location signal before converted to TDC_RISE, TDC_FALL).

With regard to claim 21, the method further comprises the steps of combining the numerical phase difference value (PHF) with a value in an accumulator (102) to obtain a new accumulator value; and presenting the new accumulator value (PHE) as a result of a phase comparison.

With regard to claim 22, the method further comprises the steps of propagating the first signal (114) through a tapped delay line (502s); latching outputs of the tapped delay line in a parallel latch (504s) in response to a transition in the second signal (110) to obtain the snapshot of the fist signal.

With regard to claims 25 and 26, controlling an output frequency (RF OUT) of an oscillator (103) using the result of the phase comparison, wherein the first signal (CKV) is an output of the oscillator (RF OUT through 106).

Claim Rejections - 35 USC § 103

Claims 8 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Staszewski et al. in view of Brachmann et al. (US 6,351,154; herein after Brachmann).

With regard to claim 8, the above discussed the apparatus of Staszewski meets all of the claimed limitations except that Staszewski does not disclose the apparatus is implemented on a single monolithic integrated circuit. Brachmann teaches in Fig. 5 a similar apparatus can be implemented as integrated circuit (column 4, lines 20-33) as recited in the claim. Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to implement that teaching with the apparatus of Brachmann for the advantage of reducing additional cost when implemented within other circuits, e.g. ASIC, PLD, FPGA, PLL etc.

Claim 18 is rejected for similar motivation; note the above discussion with regard to claim 8.

Claims 9 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Staszewski.

With regard to claims 9 and 19, the above discussed circuit of Staszewski meets all of the claimed limitations except for the intended use as implemented in a field programmable gate array. However, it is noted that the reference circuit has the ability to be used in this environment as well. It would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to implement that circuit taught by Staszewski in the field programmable gate array for the advantage of saving power consumption from the circuit.

(10) Response to Argument

In response to Appellant's arguments, with respect to the prior art rejections to claim 1, stating that Staszewski does not teach or suggest an apparatus having a transition location signal because Staszewski labels the snapshot 604 to be a timing signal, not a transition location signal as claimed. Even though Staszewski does not call 604 as a transition location signal, 604 is interpreted as claimed transition location signal. Since, the skilled artisan in the art would clearly understand that a transition location signal as the signal that corresponds to transition location of the signal FREF (110) makes its transition at each of the locations requiring the signal FREF as depicted in FIG. 6 of Staszewski et al. Thus the snapshot 604 of Staszewski clearly anticipates the transition location signal. Furthermore, the signal 604 is a transition location signal as evidenced by Appellant's acknowledgement in page 11 of the arguments (see the notes of Appellant's drawing) in which Appellant admits that 604 in Fig. 6 of Staszewski is transition location signal. Note that claim only requires a transition location signal, not specific to differentiating between rising or falling transition. Therefore, Staszewski teaches each and every recitation of claim 1 including the recitation "transition location signal".

In response to Applicant's arguments, with respect to the prior art rejections to claim 10, stating that Staszewski et al. does not disclose encoding circuitry coupled to the phase detecting stage. However, Examiner respectfully disagrees because Fig. 1 of Staszewski et al. clearly anticipates the claimed encoding circuitry coupled to the phase detecting stage (see paragraph 9 above). Furthermore, Applicant argues that the circuit (NORM) of Fig. 2 of Staszewski is not an encoding circuitry. This argument is not persuasive because one skilled in the art would recognize that an encoder generally convert an input digital signal into its equivalent binary code

(see attached copy of dictionary definition for "encoder". Note definition 7, which states "A digital device for converting an input digital signal into its equivalent binary code"). The circuit (NORM) of Fig. 2 of Staszewski is an encoding circuitry since it converts the input digital signal into its equivalent binary code (column 5, line 64 through column 6, line 43).

In response to Applicant's arguments with respect to the prior art rejections to claim 20, which is similar to claim 1. This argument is not persuasive for the same reason as discussed above.

Therefore, the rejections of record are still believed to be proper and are therefore maintained as set forth above.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

HLN
February 05, 2008

Conferees:

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